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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,139	03/12/2004	Christopher P. Duff	10040178-1	7920

7590 10/16/2008

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Intellectual Property Administration
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EXAMINER	
FLORES, LEON	

ART UNIT	PAPER NUMBER
2611	

MAIL DATE	DELIVERY MODE
10/16/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Advisory Action Before the Filing of an Appeal Brief	Application No.	Applicant(s)	
	10/799,139	DUFF ET AL.	
	Examiner	**Art Unit**	
	LEON FLORES	2611	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED _____ FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:

a) ☐ The period for reply expires _____months from the mailing date of the final rejection.

b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).

5. ☐ Applicant's reply has overcome the following rejection(s): _____.

6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

7. ☒ For purposes of appeal, the proposed amendment(s): a) ☒ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: *None*.
   Claim(s) objected to: *None*.
   Claim(s) rejected: *1-53*.
   Claim(s) withdrawn from consideration: *None*.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).

9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).

10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☐ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See continuation sheet.

12. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____

13. ☐ Other: _____.

/David C. Payne/
Supervisory Patent Examiner, Art Unit 2611

Applicant asserts that "Kirisawa provides examples of the spectrum analyzer 40's display in FIGS. 7A-7D (col. 4, line 64 - col. 5, line 5). In these displays, it is noted that there is no display of "digital interface symbol information". In fact, there is no display of any digital information at all. Although Kirisawa does illustrate waveforms containing at least some digital information in FIGS. 5A and 5B (although not digital interface symbol information), it is noted that the waveforms shown in FIGS. 5A and 5B are representative of waveforms generated by the sin ROM 23 and cos ROM 24 of the quadrature signal generator 20 (see, FIGS. 3 & 4; and col. 3, lines 60-65). The waveforms shown in FIGS. 5A and 5B are not displayed on the spectrum analyzer 40, and the waveforms shown in FIGS. 5A and 5B are not correlated with any "digital interface symbol information".
The examiner respectfully disagrees. The reference of Kirisawa teaches a calibration system comprised of quadrature phase modulator which includes a local oscillator for generating a carrier wave, a first mixer for mixing I-signal (digital data) with the carrier signal, a second mixer for mixing Q-signal (digital data) with the carrier wave, and a hybrid block for combining the output of the two mixers. One skilled in the art would know that these signals are further displayed by the spectrum analyzer. (See fig. 3 & col. 4, lines 57-61) As you can see, the concept of displaying digital data and an analog signal in a correlated fashion is not novel.

Applicant further asserts that "assume for a moment that Kirisawa does teach "displaying...at least some of the digital interface symbol information with a representation of the at least one analog signal in a correlated fashion". Even if this were so, applicant does not understand why one of ordinary skill in the art at the time of applicant's invention would have been combined Kirisawa's teachings with Jeong's".
The examiner respectfully disagrees. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, one of ordinary skills in the art would have founded obvious to combined the teachings of Jeong and Kirisawa in order to yield applicant's claimed invention.

Applicant finally asserts that "lida contains absolutely no teaching that any of the signals shown in FIGS. 2A-N are actually displayed in a correlated fashion. lida certainly does not indicate that "digital interface symbol information [captured from a set of data samples for at least one analog signal is displayed] with a representation of the set of data samples of the at least one analog signal in a correlated fashion", as is recited in applicant's claim 1".
The examiner respectfully disagrees. The reference of lida does teach displaying digital information (I & Q) correlated with an analog signal. (See figs. 2A-N & col. 6, line 39 - col. 7, line 12) As you can see, the concept of displaying digital data and an analog signal in a correlated fashion is not novel.